DATA SHEET

AAT2608

Single 800mA Switching Converter and Eight-Channel 300mA LDO Regulator

General Description

The AAT2608 is a member of Skyworks' Total Power Management IC (TPMIC™) product family. It contains an 800mA switching regulator and eight fully integrated 300mA low dropout (LDO) regulators in a small, Pb-free 28-pin 4mmx4mm TQFN package, making it ideal for space-constrained systems.

The step-down converter is a monolithic synchronous converter with an integrated compensation network and 90% efficiency. It operates at 1.5MHz and uses a tiny 2.2µH inductor with a small 10µF output capacitor. At no load the switching converter quiescent current is 70µA. The 8 channel 300mA LDO regulator features low power consumption, low dropout, and high noise immunity from the input power supply. Each channel consumes a mere 30µA of current when enabled, features 250mV of dropout at 250mA, and 68dB of power supply rejection at 10kHz. Each channel uses a small 1µF output capacitor and 2.2µF input capacitor. All regulators include a separate enable, providing a convenient solution to implement any power-up and power-down sequencing. All output voltages are factory One Time Programmable (OTP) between 0.6V and 3.7V with 100mV increment and typical regulation accuracy is ±1%. The switcher has a separate input from the linear regulators, permitting post-regulation configuration of the LDO channels from the switcher's output. Its output is externally programmable with external resistors. LDO1 and LDO2 share the same input voltage, as do LDO3 and LDO4, while LDO5 through LDO8 have their own independent input.

The AAT2608 is a safe solution which integrates an over-current limit for each channel and over-thermal protection. The device is rated over a temperature range of -40°C to 85°C.

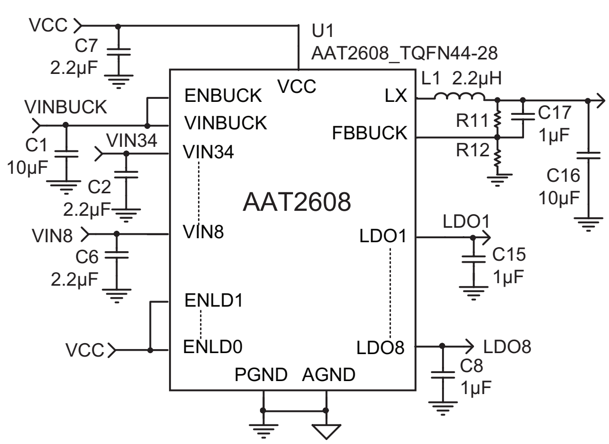
Features

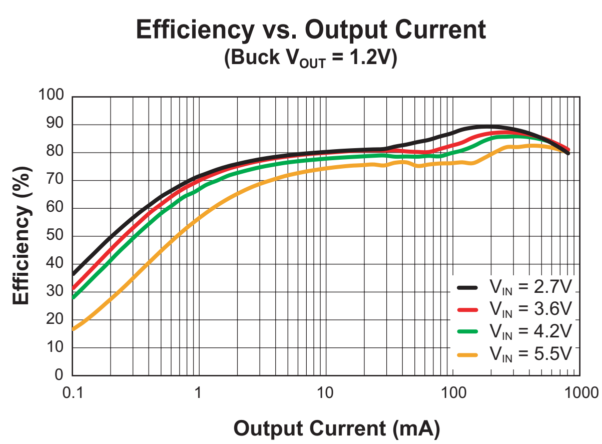
- 2.7V to 5.5V Operating Input Voltage Range
- Factory Programmable Outputs from 0.6V to 3.7V
- 800mA Monolithic Switching Converter
- 1.5MHz Switching Frequency
- 90% Efficiency
- 70µA Quiescent Current
- Independent Input Power and Ground
- Independent Enable
- ±1% Typical Accuracy
- 8 Channel 300mA LDO Regulators
- 250mV Dropout Voltage at 250mA
- Low 30µA Quiescent Current
- High PSRR (68dB @10KHZ)
- Independent Enable
- ±1% Typical Accuracy
- Over-Current Protection
- Over-Thermal Protection
- 4mmx4mm, 0.4mm Lead Pitch, 28-pin TQFN Package

Applications

- Cellular Application
- Handheld Products
- Media Players (MP4 Players)
- Portable Navigation Devices (PNDs)

Typical Application





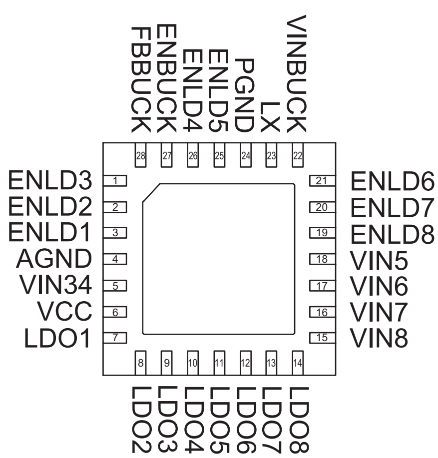
Single 800mA Switching Converter and Eight-Channel 300mA LDO Regulator

Pin Descriptions

Pin #	Symbol	Function
1	ENLD3	LDO3 enable; active high.
2	ENLD2	LDO2 enable; active high.
3	ENLD1	LDO1 enable; active high.
4	AGND	Analog ground.
5	VIN34	Input to LDO3 and LDO4.
6	VCC	Input to power control circuitry for step-down converter, bias, and LDO1 and LDO2. This pin is also the power input for LDO1 and LDO2.
7	LDO1	LDO1 output voltage.
8	LDO2	LDO2 output voltage.
9	LDO3	LDO3 output voltage.
10	LDO4	LDO4 output voltage.
11	LDO5	LDO5 output voltage.
12	LDO6	LDO6 output voltage.
13	LDO7	LDO7 output voltage.
14	LDO8	LDO8 output voltage.
15	VIN8	Input to LDO8.
16	VIN7	Input to LDO7.
17	VIN6	Input to LDO6.
18	VIN5	Input to LDO5.
19	ENLD8	LDO8 enable; active high.
20	ENLD7	LDO7 enable; active high.
21	ENLD6	LDO6 enable; active high.
22	VINBUCK	Power input to the step-down converter.
23	LX	Switching node for step-down converter.
24	PGND	Power ground for step-down converter.
25	ENLD5	LDO5 enable; active high.
26	ENLD4	LDO4 enable; active high.
27	ENBUCK	Enable for step-down converter; active high.
28	FBBUCK	Feedback input for step-down converter.

Pin Configuration

TQFN44-28
(Top View)



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Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
	VINBUCK, VCC, VIN34, VIN5, VIN6, VIN7, VIN8, ENBUCK, ENLD1, ENLD2, ENLD3, ENLD4, ENLD5, ENLD6, ENLD7, ENLD8, FBBUCK to AGND	-0.3 to 6.5	V
	LX to PGND	-0.3 to $V_{VINBUCK}$ + 0.3	V
	LDO1, LDO2 to GND	-0.3 to V_{VCC} + 0.3	V
	LDO3, LDO4 to GND	-0.3 to V_{VIN34} + 0.3	
	LDO5 to GND	-0.3 to V_{VIN5} + 0.3	
	LDO6 to GND	-0.3 to V_{VIN6} + 0.3	
	LDO7 to GND	-0.3 to V_{VIN7} + 0.3	
	LDO8 to GND	-0.3 to V_{VIN8} + 0.3	V
	PGND to AGND	-0.3 to +0.3	

Thermal Information[2]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance	50	°C/W
P_D	Maximum Power Dissipation	2	W
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.

Electrical Characteristics[1]

V_{CC} = V_{INBUCK} = V_{IN34} = V_{IN5} = V_{IN6} = V_{IN7} = V_{IN8} = V_{INLDO} = 5.0V, -40°C ≤ T_A ≤ +85°C, unless otherwise noted. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Logic Control / Protection						
V_{ENLDx} V_{ENBUCK}	Input High Threshold		1.4			V
	Input Low Threshold				0.3	V
Step-Down Converter						
V_{INBUCK}, V_{CC}	Input Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	I_{OUT} = 0mA, device switching, all LDOs disabled		70		μA
I_{SD}	Shutdown Current	ENBUCK = 0V		1		μA
$V_{O\_STEP\text{-}DOWN}$	Output Voltage Programmable Range	Using external feedback resistors	0.6		80% of V_{IN}	V
V_{REG}	Output Voltage Accuracy	0°C ≤ T_A ≤ 85°C	-3		+3	%
I_{LIM}	P-Channel Current Limit		1000			mA
$T_{STARTUP}$	Startup Time	From device enable to 90% of nominal output voltage		100		μs
T_{RAMP}	Ramp-Up Time	Time to ramp output voltage from 10% to 90%		60		μs
$R_{DS(ON)H}$	High-Side Switch On-Resistance			260		mΩ
$R_{DS(ON)L}$	Low-Side Switch On-Resistance			220		mΩ
ΔV_{OUT} / (V_{OUT} ΔV_{IN})	Line Regulation			0.2		%/V
F_{OSC}	Oscillator Frequency			1.5		MHz
UVLO	Under-Voltage Lockout Threshold	Falling		2		V
		Rising		2.2		
Low-Dropout Regulators (LDO1-LDO8)						
V_{INLDO}	Input Voltage Range		2.7		5.5	V
V_{OUTx}	LDO Output Voltage	I_{LDO} = 1mA to 300mA, OTP per requirement	0.6		V_{INLDO} - V_{DO}	V
	LDO Accuracy	I_{LDO} = 10mA	-3		+3	%
I_Q	LDO Quiescent Current	V_{INLDO} = 5V, added quiescent current when LDO is enabled		30	55	μA
	Line Regulation	I_{LDO} = 10mA		0.1		%/V
	Load Regulation	I_{LDO} = 1mA to 300mA		0.003		%/mA
	PSRR	V_{INx} = 5V, V_{OUTx} = 1.8V, EN = HIGH, F = 10KHz, I_{LDO} = 100mA		68		dB
V_{DO}	Dropout Voltage	I_{LDO} = 250mA		250	500	mV
$I_{LDO(LIM)}$	LDO Current Limit		300			mA
Thermal						
T_{SD}	Over-Temperature Shutdown Threshold	Rising		145		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			25		°C

1. Specification over the -40°C to +85°C operating temperature range is assured by design, characterization and correlation with statistical process controls.

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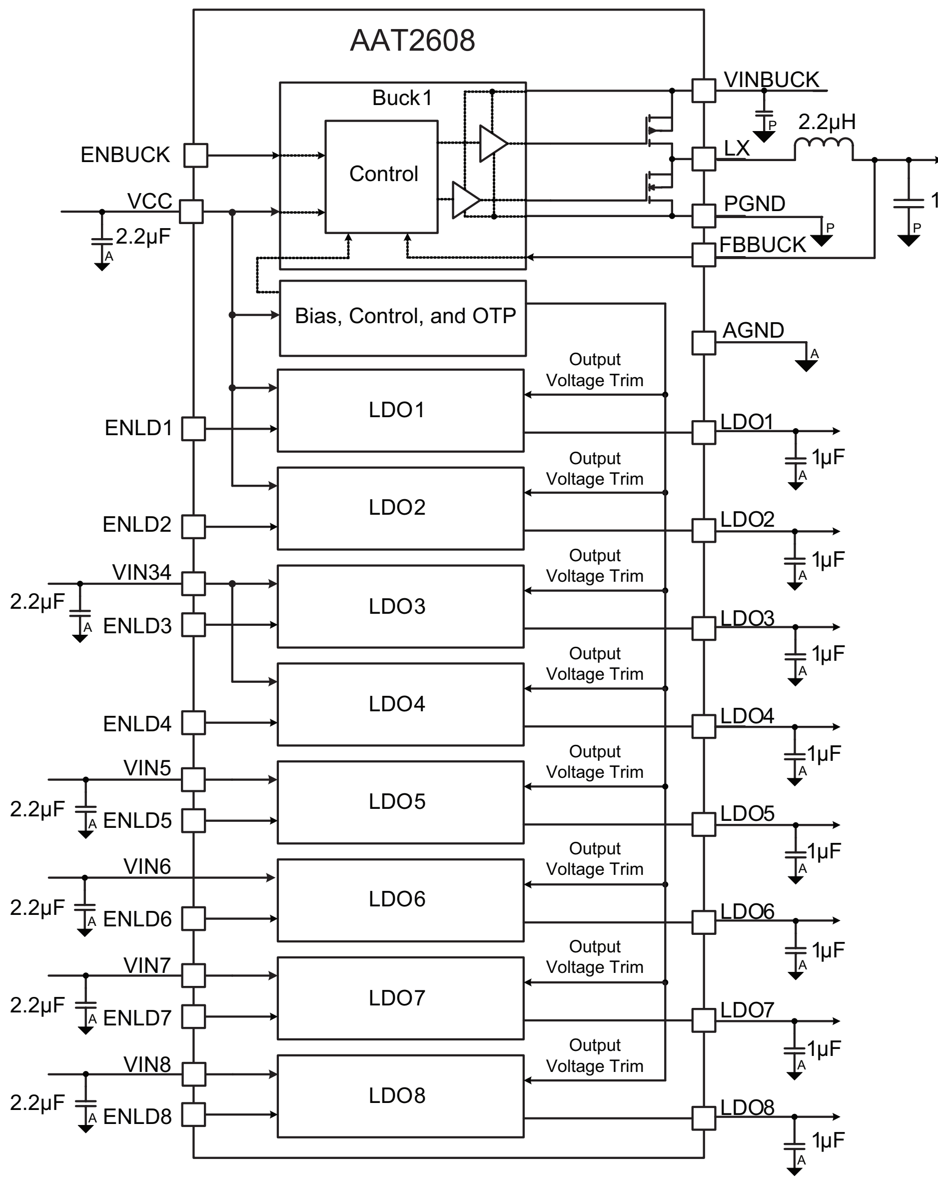
Programming Output Voltages

Programmable Output Voltage Range			Resolution
Step-down	0.6V	80% of V_{IN}	Externally Adjustable with 0.6V Internal Reference
LDO1	0.6V	3.7V	100mV
LDO2	0.6V	3.7V	100mV
LDO3	0.6V	3.7V	100mV
LDO4	0.6V	3.7V	100mV
LDO5	0.6V	3.7V	100mV
LDO6	0.6V	3.7V	100mV
LDO7	0.6V	3.7V	100mV
LDO8	0.6V	3.7V	100mV

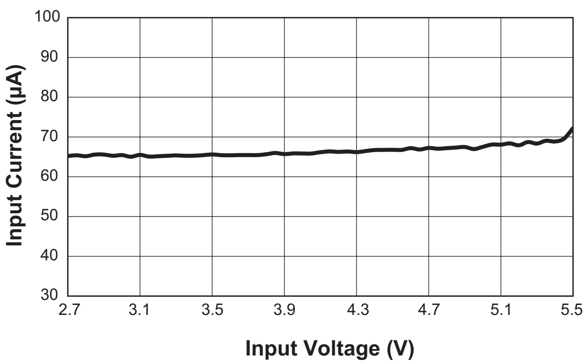
Block Diagram



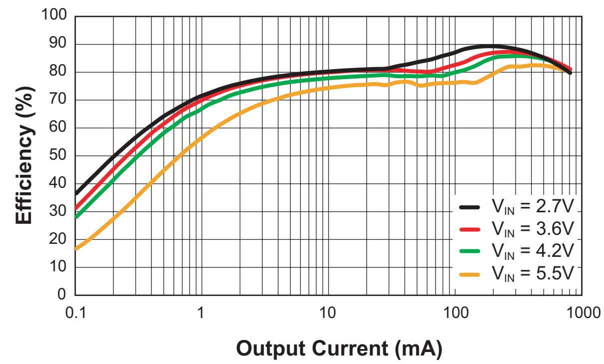
Single 800mA Switching Converter and Eight-Channel 300mA LDO Regulator

Typical Characteristics–Step-Down (Buck) Converter

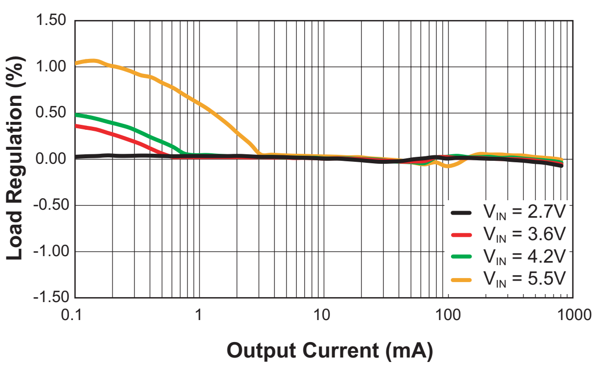
Input Current vs. Input Voltage
(Buck V_{OUT} = 1.2V; Switching; All LDOs Disabled)



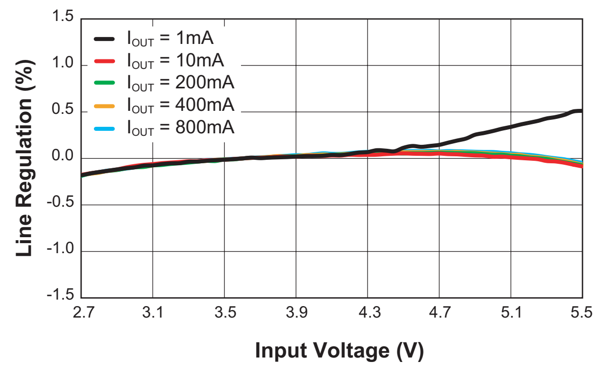
Efficiency vs. Output Current
(Buck V_{OUT} = 1.2V)



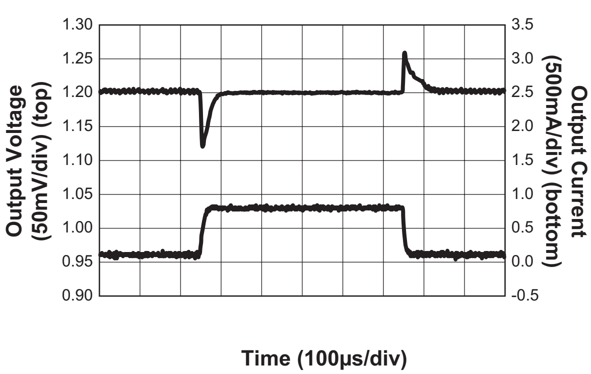
Load Regulation
(Buck V_{OUT} = 1.2V; C_{OUT} = 22µF)



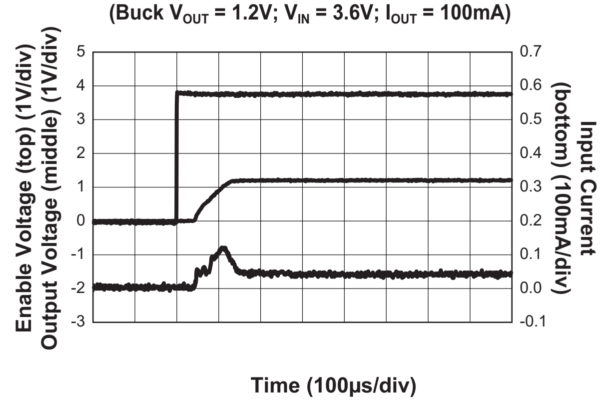
Line Regulation
(Buck V_{OUT} = 1.2V)



Load Transient
(Buck V_{OUT} = 1.2V; V_{IN} = 3.6V; I_{OUT} = 80mA to 800mA)



Soft Start
(Buck V_{OUT} = 1.2V; V_{IN} = 3.6V; I_{OUT} = 100mA)



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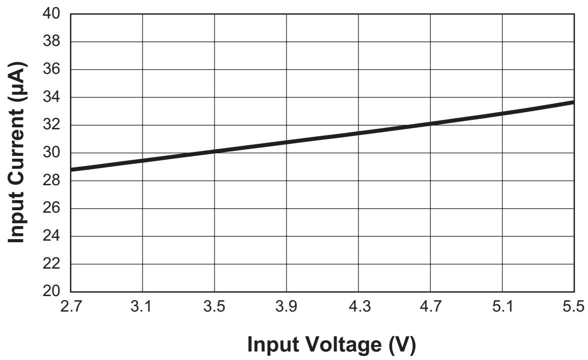
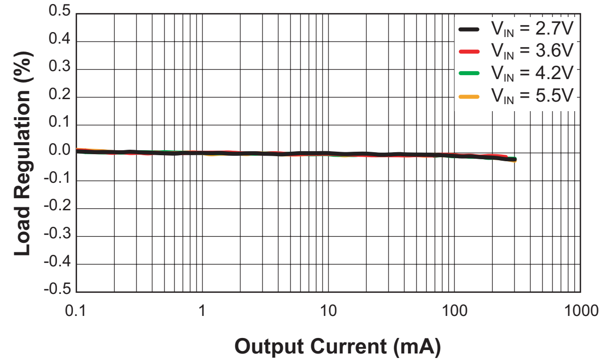
Typical Characteristics–LDO1-LDO8

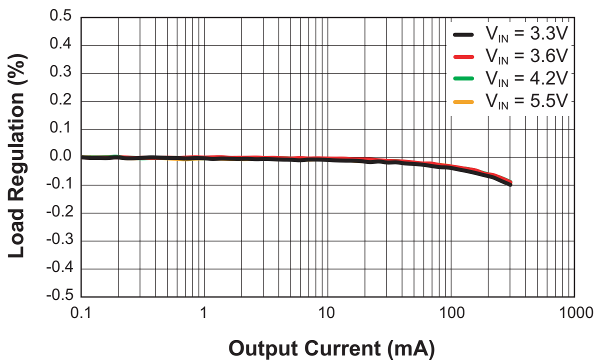
Input Current vs. Input Voltage
(Contributed By Each LDO)



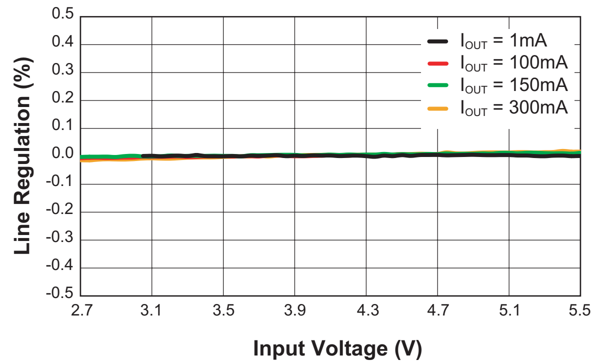
Load Regulation
(LDO1 V_{OUT} = 1.85V)



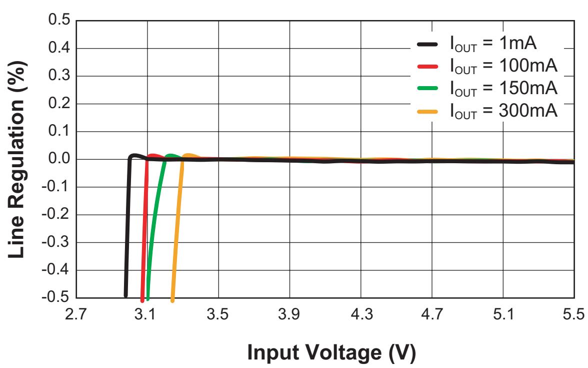
Load Regulation
(V_{OUT} = 3V)



Line Regulation
(LDO1 V_{OUT} = 1.85V)

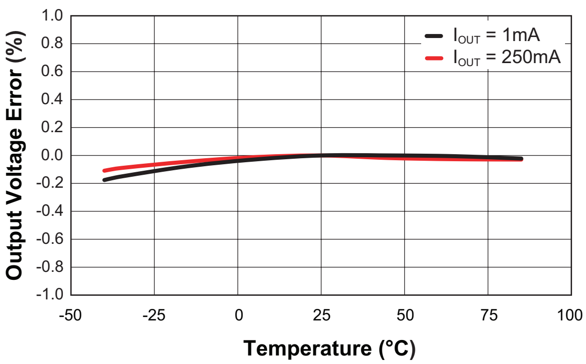


Line Regulation
(V_{OUT} = 3V)

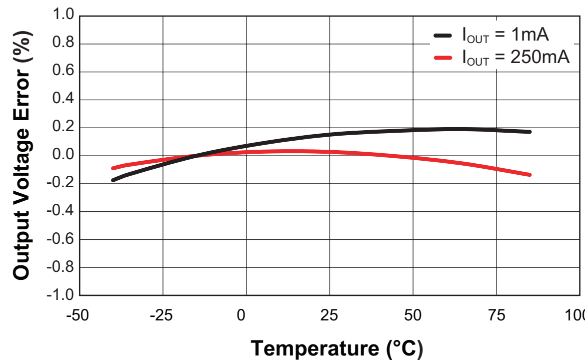


Typical Characteristics−LDO1-LDO8 (continued)

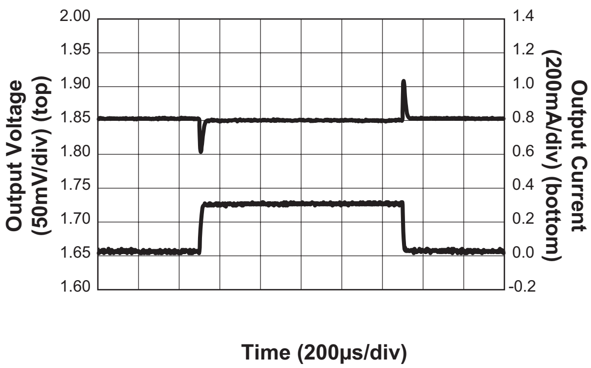
Output Voltage Error vs. Temperature
(LDO1 V_{OUT} = 1.85V; V_{IN} = 3.6V)



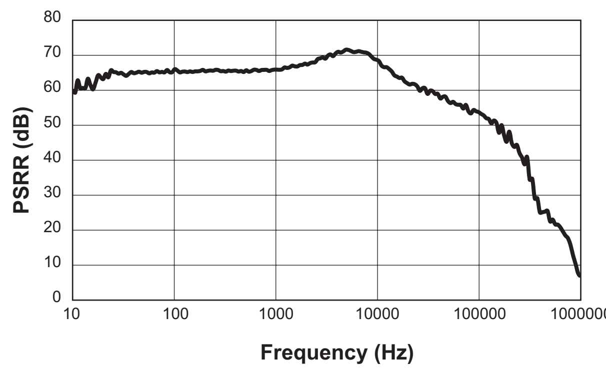
Output Voltage Error vs. Temperature
(LDO V_{OUT} = 3V)



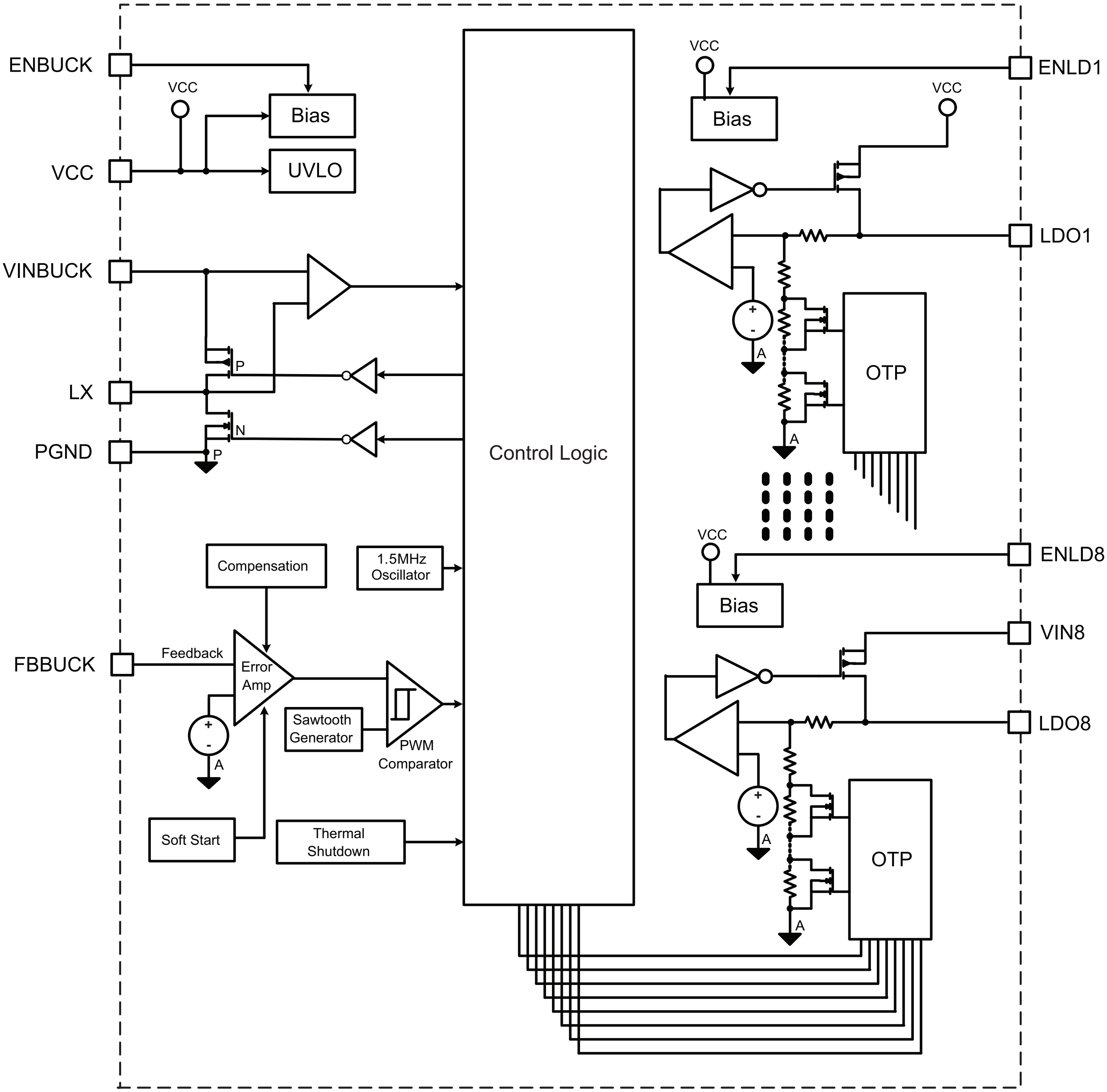
Load Transient
(LDO V_{OUT} = 1.85V; V_{IN} = 3.6V; I_{OUT} = 30mA to 300mA)



Power Supply Rejection Ratio (PSRR)
($V_{IN(DC)}$ = 5V; V_{OUT} = 1.85V; I_{OUT} = 100mA)



Functional Block Diagram



Functional Description

The AAT2608 is a highly integrated voltage regulating power management unit for mobile handsets or other portable devices. It includes an 800mA switch-mode step-down converter and eight low-noise, high-PSRR low-dropout (LDO) regulators. It operates from an input voltage between 2.7V and 5.5V making it ideal for lithium-ion or 5V regulated power sources. All nine converters have separate enable pins for ease of use.

Synchronous Step-Down (Buck) Converter

The AAT2608 switch-mode step-down converter is a constant frequency peak current mode PWM converter with internal compensation. The input voltage range is 2.7V to 5.5V. The output voltage range is 0.6V to 80% of V_{INBUCK}. The high 1.5MHz switching frequency allows the use of small external inductor and capacitor.

The step-down converter offers soft-start to limit the current surge seen at the input and eliminate output voltage overshoot. The current across the internal P-channel power switch is sensed and turns off when the current exceeds the current limit. Also, thermal protection completely disables switching if internal dissipation becomes excessive, thus protecting the device from damage. The junction over-temperature threshold is 145°C with 25°C of hysteresis.

The Buck converter is designed for a peak continuous output current of 800mA. It was designed to maintain over 80% efficiency at its maximum rated output current load of 800mA with a 1.2V output. Peak efficiency is above 90%. It also has excellent transient response, load regulation, and line regulation.

LDO Regulators

The AAT2608 includes eight LDO regulators. The regulators operate from the 2.7V to 5.5V input voltage to a regulated output voltage. Each LDO regulator has its own independent enable pin. All LDOs have a fixed output programmed during manufacturing. Each LDO consumes 30µA of quiescent current and is stable with a small 1.0µF ceramic output capacitor. These LDOs offer high power supply rejection and provide over-current and over-temperature protection.

Application Information

Synchronous Step-Down (Buck) Converter

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down-slope meets the internal slope compensation requirements. Table 1 displays suggested inductor values for various output voltages.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input; see Table 3 for suggested capacitor components. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C_{IN}. The calculated value varies with input voltage and is a maximum when V_{CC} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

For $V_{IN} = 2 * V_O$

$$I_{RMS} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{CC}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2608 step-down switching converter. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high-Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10μF to 22μF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple; see Table 2 for suggested capacitor components

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within several switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the several switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 10μF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

LDO Regulators

Input Capacitor

Typically, a 1.0μF or larger ceramic capacitor is recommended for C_{VCC}, $C_{VINBUCK}$, C_{VIN34}, C_{VIN5}, C_{VIN6}, C_{VIN7}, and C_{VIN8} in most applications. The input capacitor should be located as close to the inputs of the device as practically possible. C_{VCC}, $C_{VINBUCK}$, C_{VIN34}, C_{VIN5}, C_{VIN6}, C_{VIN7}, and C_{VIN8} values greater than 1.0μF will offer superior input line transient response and will assist in maximizing power supply ripple rejection.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between the LDOx and AGND pins. The C_{OUTx} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

The AAT2608's LDO regulators have been specifically designed to function with very low ESR ceramic capacitors. Although the device is intended to operate with these low ESR capacitors, it is stable over a very wide range of capacitor ESR, thus it will also work with higher ESR tantalum or aluminum electrolytic capacitors. However, for best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1μF to 10μF.

Thermal Calculations

There are three types of losses associated with the AAT2608 total power management solution (one step-down converter and eight LDO regulators): switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the internal power switches/FETs of the step-down converter and the power loss associated with the voltage difference across the pass switch/FET of the eight LDO regulators. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by the following (quiescent and switching losses are ignored, since conduction losses are so dominant):

$$P_B = \frac{I_{OB}^2 \cdot (R_{DS(ON)H} \cdot V_{OB} + R_{DS(ON)L} \cdot [V_{INBUCK} - V_{OB}])}{V_{IN}}$$

$$P_{LDO1} = I_{LDO1} \cdot (V_{CC} - V_{OL1})$$

$$P_{LDO2} = I_{LDO2} \cdot (V_{CC} - V_{OL2})$$

$$P_{LDO3} = I_{LDO3} \cdot (V_{IN34} - V_{OL3})$$

$$P_{LDO4} = I_{LDO4} \cdot (V_{IN34} - V_{OL4})$$

$$P_{LDO5} = I_{LDO5} \cdot (V_{IN5} - V_{OL5})$$

$$P_{LDO6} = I_{LDO6} \cdot (V_{IN6} - V_{OL6})$$

$$P_{LDO7} = I_{LDO7} \cdot (V_{IN7} - V_{OL7})$$

$$P_{LDO8} = I_{LDO8} \cdot (V_{IN8} - V_{OL8})$$

$$P_{TOTAL} = P_B + P_{LDO1} + P_{LDO2} + P_{LDO3} + P_{LDO4} + P_{LDO5} + P_{LDO6} + P_{LDO7} + P_{LDO8}$$

P_B: Power dissipation of the DC-DC regulator
I_{OB}: Output current of the specific DC-DC regulator
$R_{DS(ON)H}$: Resistance of the internal high-side switch/FET
$R_{DS(ON)L}$: Resistance of the internal low-side switch/FET
V_{OB}: Output voltage of the DC-DC regulator
V_{CC}: Input voltage of the DC-DC regulator, LDO1, and LDO2
P_{LDOx}: Power dissipation of the specific LDO regulator
I_{LDOx}: Output current of the specific LDO regulator
V_{INBUCK}: Input voltage of the step-down converter.
V_{IN34}: Input voltage of LDO3 and LDO4
V_{IN5}: Input voltage of LDO5
V_{IN6}: Input voltage of LDO6
V_{IN7}: Input voltage of LDO7
V_{IN8}: Input voltage of LDO8
V_{OLx}: Output voltage of the specific LDO regulator
P_{TOTAL}: Total power dissipation of the AAT2608

Since $R_{DS(ON)}$ and conduction losses all vary with input voltage, the dominant losses should be investigated over the complete input voltage range. Given the total conduction losses, the maximum junction temperature (125°C) can be derived from the θ_{JA} for the TQFN44-28 package which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \theta_{JA} + T_A$$

$T_{J(MAX)} = P_{TOTAL} \cdot \theta_{JA} + T_A$
$T_{J(MAX)}$: Maximum junction temperature
P_{TOTAL}: Total conduction losses
Θ_{JA}: Thermal impedance of the package
T_A: Ambient temperature

Layout

The suggested PCB layout for the AAT2608 is shown in Figures 2 and 3. The following guidelines should be used to help ensure a proper layout.

1. The input capacitors (C1, C2, C3, C4, C5, C6) should connect as closely as possible to VINBUCK (Pin 22), VIN34 (Pin 5), VIN5 (Pin 18), VIN6 (Pin 17), VIN7 (Pin 16) VIN8 (Pin 15), VCC (Pin 6), and AGND/PGND (Pins 4 and 24).
2. C13 (the step-down converter output capacitor) and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible.
3. The feedback trace or FBBUCK pin (Pin 28) should be separated from any power trace and connected as closely as possible to the load point. Sensing along a high current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FBBUCK pin (Pin 28) to minimize the length of the high impedance feedback trace.
4. The resistance of the trace from the load return to the PGND (Pin 24) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. For good thermal coupling, PCB vias are required from the pad for the TQFN44-28 exposed paddle to the ground plane.

Manufacturer	Part Number/ Type	Inductance (μH)	Rated Current (A)	DCR (mΩ) (max)	Size (mm) LxWxH
TDK	LTF5022	1.2	4.3	25	5x5.2x2.2
		1.8	3.6	32	
		2.2	3.2	40	
		3.3	2.5	60	
Wurth Electronik	WE-TPC Type M	1	2.6	30	4.8x4.8x1.8
		1.8	2.35	50	
		2.7	2.03	60	
		3.3	1.8	65	
	WE-TPC Type MH	1.2	2.8	20	4.8x4.8x2.8
		1.8	2.45	25	
		2.2	2.35	28	
		2.7	1.95	30	
		3.3	1.8	35	
Murata	LQH55D	1	4	19 (typ)	5x5.7x4.7
		1.5	3.7	22 (typ)	
		2.2	3.2	29 (typ)	
		3.3	2.9	36 (typ)	

Table 1: Suggested Inductor Components.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
AVX	0603ZD105K	1μF	10	X5R	0603
	0603ZD225K	2.2μF	10		
TDK	C1608X5R1E105K	1μF	25	X5R	0603
	C1608X5R1C225K	2.2μF	16		
	C1608X5R1A475K	4.7μF	10		
	C2012X5R1A106K	10μF	10		0805
	C3216X5R1A226K	22μF	10		1206
Murata	GRM188R61C105K	1μF	16	X5R	0603
	GRM188R61A225K	2.2μF	10		
	GRM219R61A106K	10μF	10		0805
	GRM31CR71A226K	22μF	10	X7R	1206
Taiyo Yuden	LMK107BJ475KA	4.7μF	10	X5R	0603

Table 2: Suggested Capacitor Components.

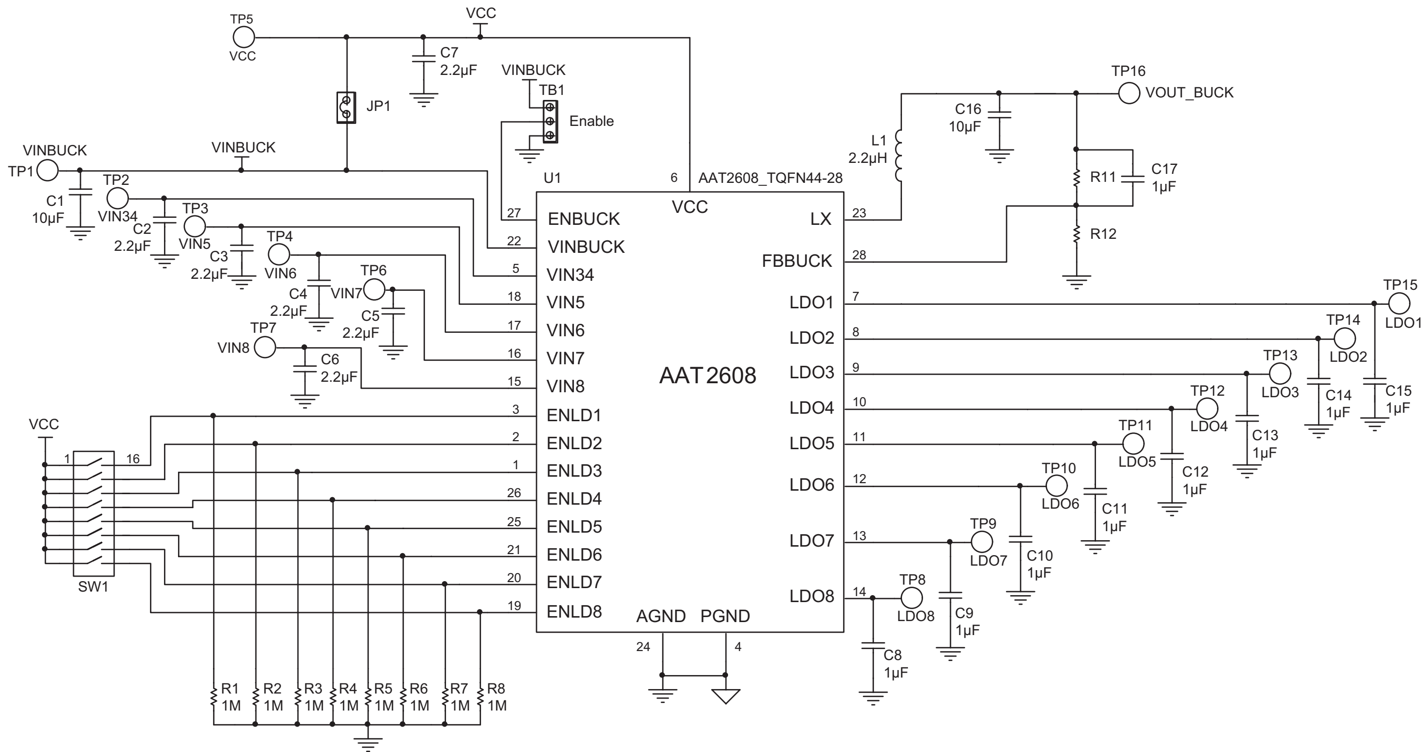


Figure 1: AAT2608 Evaluation Board Schematic.

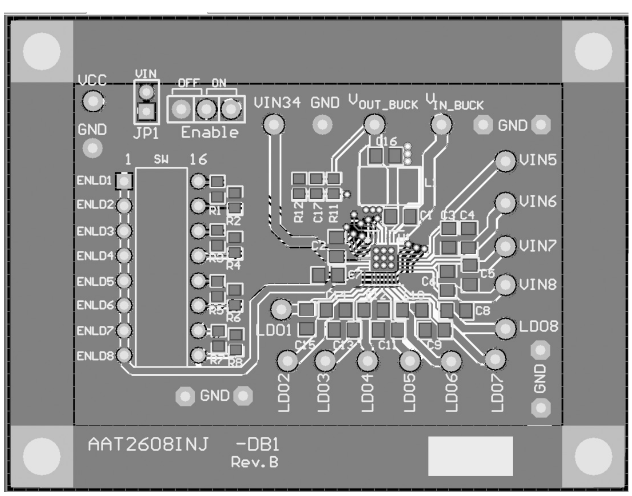


Figure 2: AAT2608 Evaluation Board Top Side PCB Layout.

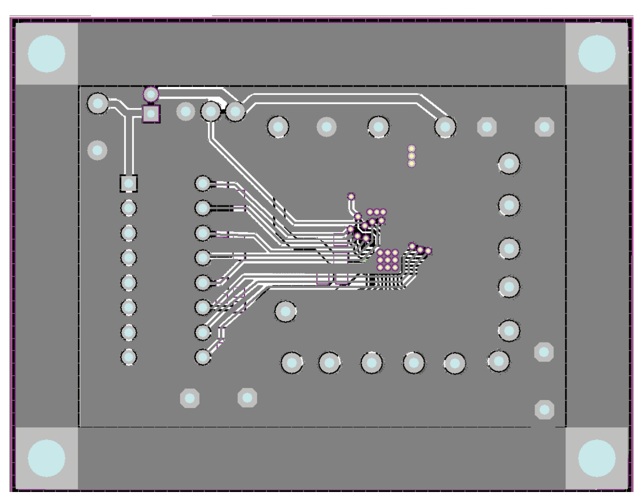


Figure 3: AAT2608 Evaluation Board Bottom Side PCB Layout.

Single 800mA Switching Converter and Eight-Channel 300mA LDO Regulator

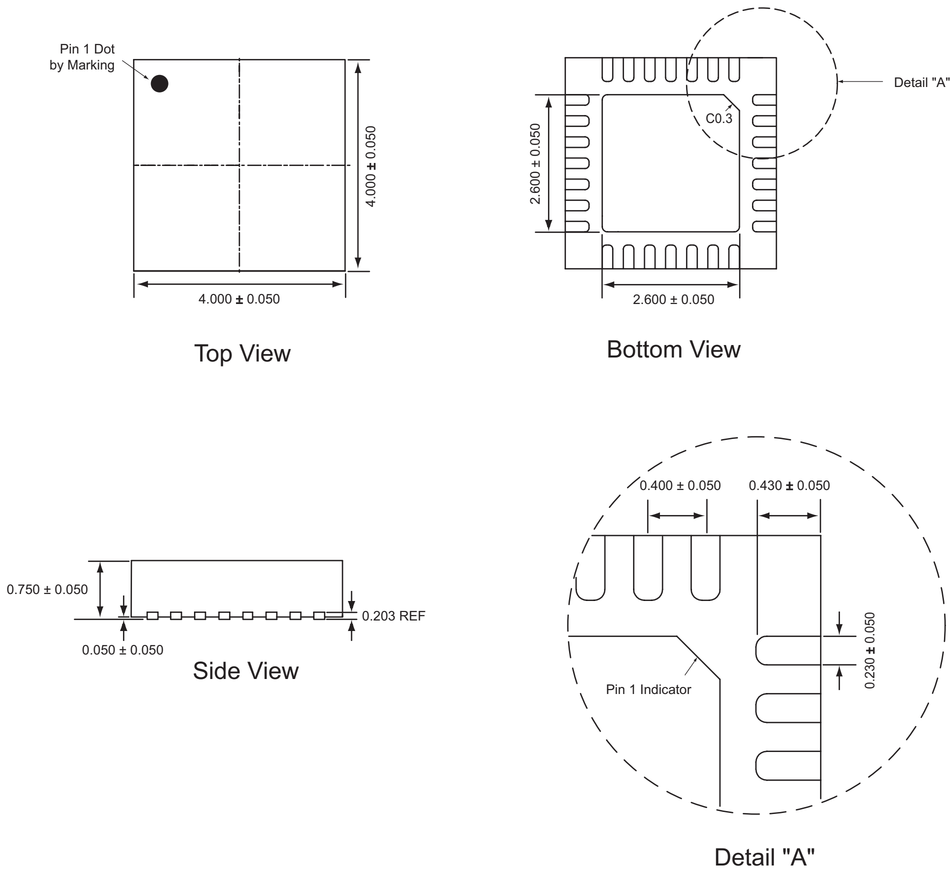
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TQFN44-28	9QXYY	**AAT2608INJ-1-T1**

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Package Information[3]

TQFN44-28



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.